Development of a Readout Technique for the High Data Rate BTeV Pixel Detector at Fermilab

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***Abstract*—The pixel detector for the BTeV experiment at Fermilab provides digitized data from approximately 22 million silicon pixel channels. Portions of the detector are six millimeters from the beam providing a substantial hit rate and high radiation dose. The pixel detector data will be employed by the lowest level trigger system for track reconstruction every beam crossing. These requirements impose a considerable constraint on the readout scheme. This paper presents a readout technique that provides the bandwidth that is adequate for high hit rates, minimizes the number of radiation hard components, and satisfies all other design constraints.**

I. Introduction

The pixel detector system for the BTeV experiment at Fermilab consists of approximately 22 million channels of 50μm × 400μm pixel sensors [1]. The silicon pixel sensors are bump bonded to Fermilab Pixel (FPIX) readout chips where each chip bonds to an array of 128×22 sensors and are placed as close as 6mm from the beam center. High density multilayer flex circuits are used to assemble the FPIX chips into modules consisting of differing numbers of chips [2]. The flex circuits provide the data path from each FPIX chip to a vacuum feedthrough board. This vacuum feedthrough board allows the FPIX chip signals to be routed to a header outside the vacuum connecting a cable that brings the signals to a Pixel Data Combiner Board (PDCB) approximately 10m away.

The pixel detector system consists of 30 pixel stations with each station spaced 1.65" apart. A single pixel station is shown in Figure 1. The stations consist of four types of sensor modules, bonded to 4, 5, 6, or 8 FPIX readout chips. Modules of 8 chips are read out using two 4-chip high density flex circuits. A station is instrumented on both sides with the opposite orientation of the pixel sensors and a 12mm wide opening in the middle to accommodate the beam. There is a total of 174 FPIX chips on the bend view side and a total of 80 chips on the non-bend view side.

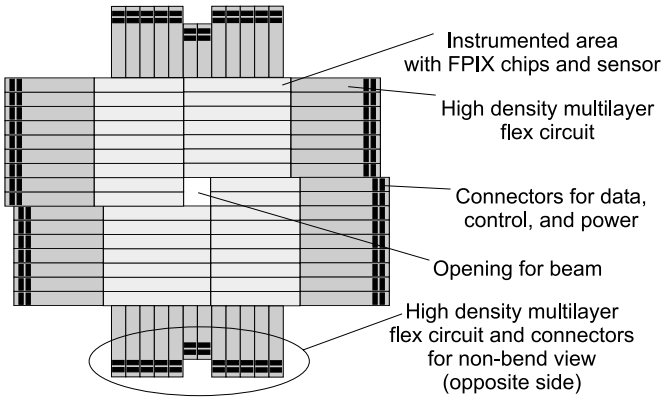

Fig. 1. Anatomy of a pixel station. Bend-view side is shown.

The FPIX chip can be broken into two distinct functional sections: the core and the periphery. The FPIX core has been in development since 1997 and has been extensively prototyped and tested [3]. The core provides a 23 bit word for every pixel hit consisting of a 3 bit pulse height ADC, 8 bit bunch crossing number, 5 bit column address (columns 0 to 21) and 7 bit row address (rows 0 to 127). The challenge of the readout scheme is in the design of the periphery. The periphery needs to move the data out of the core, off the chip onto the flex circuit, to the feedthrough board, to data cables outside the vacuum and finally to PDCB 10m away.

II. Simulations

In order to design an appropriate readout system for the pixel detector, a study to understand the bandwidth requirements was undertaken. The physics simulation tool GEANT was used to generate expected hits over a pixel station. This hit information was then used to determine the bandwidth requirements for each FPIX chip on a pixel station. Figure 2 shows the results for a worst case module (module closest to the beam) at 3x the expected nominal luminosity. This figure shows that the readout solution must accommodate Chip 1's average data rate of 684Mbps as well as Chip 6's much lower rate of 35Mbps. This large discrepancy in bandwidth requirements is exploited in the design solution described in section IV.

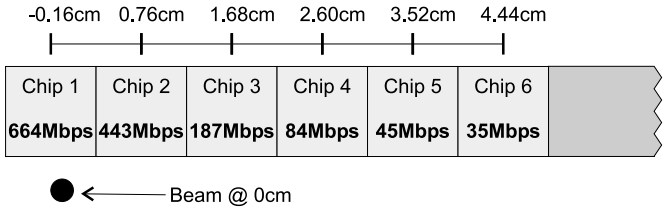

Fig. 2. Average data rates out of FPIX cores for worst case module based on simulated data at 3x expected nominal luminosity.

Simulations have shown that the maximum core clock frequency is 34.7MHz. Given this core clock frequency, the readout efficiency of Chip 1 at nominal luminosity is 99.8%. Even at three times the nominal luminosity, the efficiency of the core of Chip 1 is 98.0%. Efficiency is lost either due to a pixel being hit more than once before the first hit can be readout, or due to bottlenecks in the core circuitry.

Other studies show that this efficiency is adequate for accurate track reconstruction at the BTeV trigger system. This implies that Chip 1 shown in Figure 2 will need to operate at its maximum operating frequency to maintain 98% efficiency, however, the remaining chips likely can operate at a much slower core frequency and still maintain a high efficiency due to their low hit rates.

III. Design Constraints

The BTeV pixel detector environment in which the readout scheme must operate offers many design challenges. These constraints are outlined in this section.

A. High Radiation Area

The proximity of the pixel detector to the beam is a close a 6mm. The radiation at this proximity makes the use of PLLs and other radiation sensitive circuits unattractive. It also implies that if any additional components (other than FPIX) are to be used in the readout scheme, they will have to be radiation-hard ASICs.

B. Inaccessible Area

The pixel detector is inside a vacuum chamber which itself is inside a magnet and very difficult to physically access. This is motivation for a solution that offers high reliability.

C. Maximum Flex Circuit Width

The construction of the multichip flex circuit module requires that the width be constrained so that it does not interfere with the adjacent module. The width of the flex circuit can be minimized by minimizing the amount of data lines. Minimizing the data lines also gives the option of relaxing the design rules in the construction of the flex circuit.

D. Minimize Connectors and Cabling

Connectors and cabling inside and outside the vacuum vessel will be a mechanical challenge to accommodate. Reducing the number of data lines also reduces the amount of cabling and connectors required making the cable routing design easier and less expensive.

E. High Readout Efficiency Required

Data for the pixel detector will be used in BTeV's lowest level trigger. The trigger will reconstruct tracks and requires a high efficiency in the data. The simulations have shown that the worst case chip (Chip 1 in Figure 2) does have an adequate efficiency out of the core when operating at maximum frequency. However, any additional inefficiency would significantly reduce the BTeV trigger efficiency. This implies that there should be not additional loss in readout efficiency due the readout scheme.

F. Data Driven 10 meters

The distance from the FPIX chips to the PDCB is approximately 10m. In additional, the data needs to pass through connectors and the feedthrough board. This makes very high switching frequencies and single ended signaling levels unattractive.

IV. Design Solution

The design constraints outlined in the previous section have to be met in order to provide a successful readout scheme for the BTeV pixel detector. To address the reliability issue, it was decided that all data paths should be point to point. This allows a single FPIX to have a failure while not affecting any other chips as well as eliminating the need to embed a chip ID in the data. In addition, it was decided that no other active components should be present on the module except for the FPIX chips themselves. This eliminates time and expense of developing another chip and introducing an additional failure point in the system.

Since the data has to travel approximately 10m, the FPIX chip uses LVDS to drive and receive all signals. While this increases the number of traces on the flex circuit, this disadvantage is more than offset by the fact that LVDS signal can be driven 10m, provide excellent common mode noise rejection, and can be received by commercially available FPGAs.

Conceptually, the easiest way to move the 23 bit wide data out of the FPIX core through the FPIX periphery and onto the flex circuit is to simply drive the data in parallel. This however, would cause far too many data lines on the flex circuit and violate the maximum flex circuit width design constraint as well as the constraint to minimize the data cables and connectors. This technique would also provide much greater bandwidth than required by the low occupancy chips.

The other extreme is serialize the 23 bit word utilizing a single serial line. This however, would require a FPIX chip operating at full speed to serialize 23 bits at 34.7Mhz resulting in a 798Mbps serial link not including extra bits for DC balancing the line and/or other data encoding. A data link this fast would require a large design effort and would likely not meet the reliability design constraints. As with the 23 bit wide parallel readout, low occupancy chips would have a data path that far exceeds the bandwidth requirement.

The design solution is a compromise of these two extremes.

A. Configurable Number of Serial Lines

The main feature of BTeV pixel detector design solution is a configurable FPIX that serializes the core data utilizing either 6, 4, 2, or 1 serializers. The 6 serializer configuration is used to accommodate the high occupancy chips (such as Chip 1 in Figure 2) while the 4, 2, and 1 serializer configuration are used to accommodate the lower occupancy chips. With 6 serializers, the FPIX core is allowed to operate at its maximum operating frequency. With a core clock operating frequency of 34.7Mhz the 6 serializers each serialize 4 bits every 34.7Mhz. One extra bit is added to the 23 bit word as described in the next section for a total of 24 bits. This requires each of the 6 serial links to operate at 138.8Mbps.

For the other serial configurations, the individual serial link data rates remain at 138.8Mbps, but the FPIX core clock is proportionately reduced to match the bandwidth of the serializer configuration. To avoid multiple versions of the FPIX chip they will be configurable via a configuration register accessible through the control interface.

Table 1 summarizes the four different configurations and their respective parameters. The core clock frequency is a division of the serializer frequency (138.8Mhz in all four configurations) by the number of bits serialized by each serializer. By matching the core bandwidth to the serializer bandwidth (minus one bit), no data buffering is required after the core. Being able to configure FPIX to either utilize 6, 4, 2, or 1 serializers allows for better optimization of the number of data lines used in the complete readout system.

The optimal FPIX configuration is a configuration with the fewest number of serializers while maintaining a high readout efficiency. Simulations were run on a Verilog model of the FPIX core to determine the optimal FPIX configurations. Simulated hits were fed into the Verilog model while exercising the core at each of the four possible core clock frequencies. Figure 3 shows the optimal FPIX configurations and their readout efficiencies for the worst case module.

TABLE I
FPIX CONFIGURATIONS

Number of Serializers	Number of Bits Serialized by Each Serializer Every Core Clock Cycle	Serializer Frequency (MHz)	Core Clock Frequency (MHz)	Readout Bandwidth (Mbps)
6	4	138.8	34.7	833
4	6	138.8	23.1	555
2	12	138.8	11.6	278
1	24	138.8	5.8	139

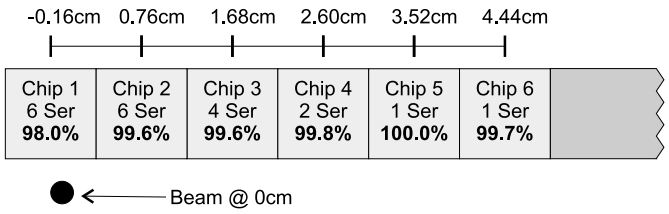

Fig. 3. Core readout efficiency and FPIX configurations for worst case module at 3x nominal luminosity.

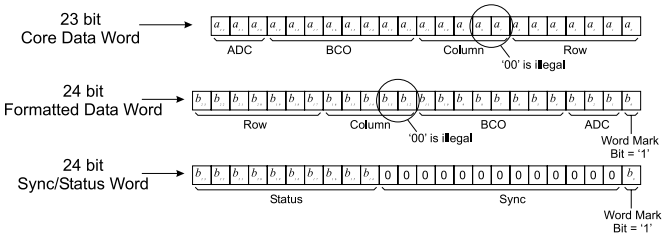

Fig. 4. Core data word and 24 bit words created by the periphery for serialization.

B. Data Word Alignment

The periphery modifies the core data word into a 24 bit formatted data word (see Figure 4). The modification includes the addition of a word mark bit in the least significant bit position and rearrangement of the row address, column address, BCO (bunch crossing) number, and ADC within the word. Static registers in the core set the five bit column address and are designed to guarantee the two least significant bits to never be '00'. This allows the sync/status word to have a unique sequence of 14 bits that is a '1' followed by thirteen '0's. Because of the arrangement of the formatted data word and the illegal '00' in the two least significant bits of the column address this 14 bit sequence is impossible to appear in any formatted data word or back to back formatted data words. The receiver uses the sync/status word to establish the word boundaries at startup and reestablish if bits are lost during data transmission. The periphery transmits a sync/status word when the core has no data and each time that the core completes an internal token passing sweep through its entire array.

This simple data alignment technique requires no handshaking between the receiver on the PDCB and the FPIX chip. If data bits are dropped during transmission, the receiver will not properly recognize where the word boundary is, but will re-sync after receiving the next sync/status word.

The leading word mark bit serves two purposes for the data receiver. Firstly, it is part of the sync/status word that contains a unique sequence of bits that can only appear in a sync/status word and secondly, it is used as a check that guarantees a '1' every 24 received bits.

The 10 status bits in the sync/status word are used to send any FPIX status flags back to the receiver FPGA and BTeV DAQ system.

C. Clock Delivery and Data Latch Clock Return

Two clocks 90° out of phase and ½ the serialization clock frequency are transmitted to FPIX. FPIX XORs these two clocks inside the FPIX chip to produce the internal serialization clock at 138.8Mhz. The recovered serialization clock is then divided down to create the FPIX chip core clock. The degree of division depends on the particular FPIX chip serialization configuration as described in Table 1.

Using a two phase clock transmission technique has many advantages. It is very simple for FPIX to recover a serialization clock with a single XOR gate. This requires no analog delays for clock doubling, allows the switching frequency on the data cable to be ½ the serialization clock

frequency, allows the serialization clock to easily scale up or down in frequency, and gives the PDCB fine control over the duty cycle of the recovered serialization clock.

To give the receiving FPGA a reliable way of latching in the incoming serial data, each FPIX chip sends a Data Latch Clock (DLCLK) in parallel with its own serialized data. DLCLK is half the serialization clock frequency and its edges are half way between the edges of the data. This allows for maximum setup and hold at the receiver FPGA flip-flops. Data recovery at the FPGA uses both edges of the DLCLK to latch in bits on the incoming serial data streams. Since the DLCLK is always between data transitions, there is no need for external analog delays to align the DLCLK with the data. The incoming serial data is clocked into serial shift registers where the word mark bit is used to check the boundaries of the 24 bit words.

By making the DLCLK sensitive to the falling edge of the serialization clock and the serializers sensitive to the rising edge, the PDCB has good control of the alignment of DLCLK to the serialized data.

Figure 5 shows the signals for the worst case module. Note that the two clocks and control signals are bussed to each FPIX chip while the data paths are point to point. Figure 6 and 7 are example waveforms for the 2 serializer and 6 serializer configuration, respectively.

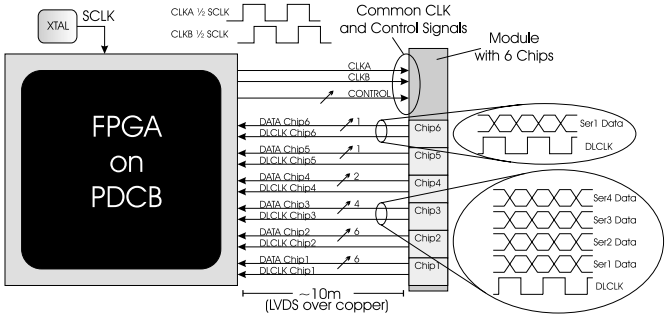

Fig. 5. Worst case module signals showing bussed clocks and control and point to point data paths.

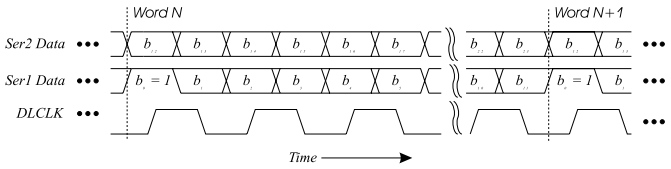

Fig. 6. Waveforms for 2 serializer configuration.

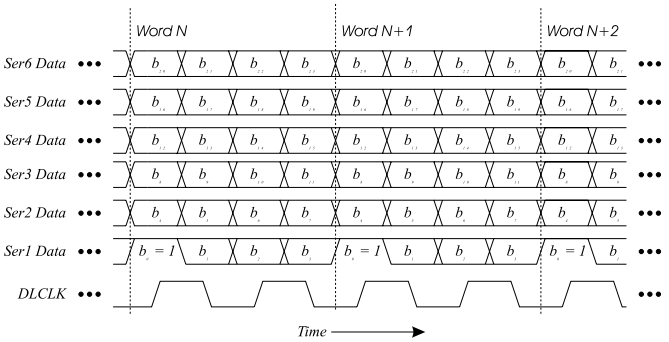

Fig. 7. Waveforms for 6 serializer configuration.

TABLE II. TABLE OF SYSTEM TOTALS

Parameter	Value
Number of FPIX chips configured with 6 serializers per station	18
Number of FPIX chips configured with 4 serializers per station	28
Number of FPIX chips configured with 2 serializers per station	66
Number of FPIX chips configured with 1 serializers per station	142
Data readout bandwidth per station	68.6 Gbps
Data readout bandwidth for BTeV pixel detector system	2 Tbps

V. SUMMARY

Table 2 summarizes the BTeV pixel readout system. The readout solution provides four possible FPIX configurations with a total a bandwidth 68.6 Gbps per station and 2 Tbps over the entire system.

The readout technique offers a simple and reliable solution to the design constraints imposed by the experiment. The clock and data alignment technique allows for a reliable design that doesn't rely on phase locked loops, analog delays or other radiation hard components. The point to point data links minimizes the risk of an entire module failure due to a single chip failure and eliminates the need for a chip ID to be embedded in the data stream. Simulations have shown that this readout scheme results in readout efficiencies that are sufficient for the BTeV experiment.

VI. REFERENCES

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